REMARKS

Claims 1-10, 17, and 18 are pending. Claims 4 and 6 have been amended. Claims 17, 18 have been added. Applicant reserves the right to pursue the original claims and other claims in this and in other applications.

Claims 1-10 stand objected to because of informalities. Specifically, the limitation "analog circuit" of claim 1 and the limitation "the specific material of the resistive element" of claims 4 and 6 are deemed unclear. Claims 4 and 6 have been amended to overcome the objection. With respect to the term "analog circuit," it is well known that such circuits process signals which may continuously vary in level, as compared with digital circuit which handle signals which vary between typically two discrete levels.

Claims 1-2 and 4-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,972,756 ("Kono"). Applicant respectfully traverses the rejection.

Claim 1 recites a semiconductor apparatus and recites, in part, "an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material."

Kono is directed to a method of fabricating a semiconductor memory device with a fuse portion. (Kono, Abstract). The Office Action points to Kono Fig. 11 as an anticipation of claims 1, 2, and 4-7. Although the Kono device may have a substrate 102 and an electrode pad 106, it does not disclose "an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material." Instead, Kono discloses an insulating film 143 under an electrode pad 146 which is provided over the periphery circuitry area

102b of the disclosed memory device. (Kono, col. 6, lines 55-60). The periphery of a memory device is a digital circuit area. There is no disclosure of an "analog circuit formed in a region under the electrode pad," much less one "comprising a resistive element including a semiconductor material." The Office Action also points to bit line 122 as the claimed resistive element. This element is not formed in a region under electrode pad 106, but is instead formed in the memory array area 101a which is not under electrode pad 106. Moreover, the Kono device does not have a resistive element in the memory array area 101a but rather a bit line 122, which is a conductor connected to a source/drain region 106b. (Kono, col. 6, lines 5-15). Because Kono does not disclose, teach or suggest all of the limitations of claim 1, Applicant respectfully submits that the 35 U.S.C. § 102(b) rejection of independent claim 1 and dependent claims 2, and 4-7 be withdrawn and the claims allowed.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,806,536 ("Gris"). Applicant respectfully traverses the rejection.

Claim 1 recites a semiconductor apparatus and recites, in part, "an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material."

Gris is directed to composite electronic chips that perform multiple functions. (Gris, Abstract; col. 1, lines 8-10). Although the Gris device may have a substrate and an electrode pad 24, it does not disclose "an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material." Instead, Gris discloses a resistance element R (Fig. 6) in a region laterally removed from beneath the electrode pad 24. There is no "analog circuit" beneath pad 24, much less one "comprising a resistive element including a semiconductor material." Because Gris does not disclose, teach or suggest

all of the limitations of claim 1, Applicant respectfully submits that the 35 U.S.C. § 102(e) rejection of claim 1 be withdrawn and the claim allowed.

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Published Application 2002/0000671 ("Zuniga") in view of U.S. Patent No. 5,489,547 ("Erdeljac"). Applicant respectfully traverses the rejection.

Claim 1 recites a semiconductor apparatus and recites, in part, "an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material."

Zuniga is directed to an architecture and method of fabrication for an integrated circuit that permit wire bonding to be performed directly over portions of the active circuit area. (Zuniga, Abstract). Zuniga may have a substrate 701, an electrode pad 512, and a MOS transistor but it does not disclose, teach or suggest "an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material." Instead, Zuniga discloses a metal layer 512 and 513 making contact with a CMOS transistor. (Zuniga, ¶¶ [0051]-[0052]). Additionally, Zuniga does not disclose an "analog circuit" formed under an electrode pad, much less one "comprising a resistive element including a semiconductor material."

Erdeljac does not supplement the deficiencies of Zuniga. Erdeljac is relied on to teach an integrated circuit device having polysilicon resistors. In fact, Erdeljac is directed to a method of fabrication of a semiconductor device and a device having a polysilicon resistor with a low temperature coefficient. (Erdeljac, col. 1, lines 7-10). Erdeljac does not disclose, teach or suggest "an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material." Moreover, even if the Erdeljac resistors were

used in Zuniga, they would still not be in a region of Zuniga under the electrode pad 512 as there is no "analog circuit" in Zuniga under electrode pad 512. Because cited references, individually or in combination, fail to teach or suggest all of the elements of claim 1, Applicant respectfully requests the rejection of independent claim 1 and dependent claims 2-4 be withdrawn.

Zuniga and Erdeljac are also not properly combinable for the purpose of an obviousness rejection. There is no motivation to combine the references to allow the invention defined by claim 1 absent the improper and impermissible use of hindsight using the present application as a roadmap. The mere fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness, the prior art must also suggest the desirability of the combination, which is not present here. M.P.E.P. § 2143.01 (citing In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990) (emphasis added). There is simply no suggestion for the proposed combination in the references, M.P.E.P. § 2141.01(III) and, in any event, the combination still does not attain the subject matter of the invention.

Claims 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kono in view of U.S. Patent No. 6,232,823 ("Tsuchida"). Applicant respectfully traverses the rejection.

Claims 9 depends from claim 1 and claims 8 and 10 ultimately depend from claim 1 and thus, include all of the limitations of claim 1. As such, claims 8-10 recite, in part, "an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material." As mentioned earlier, Kono fails to teach this limitation. Tsuchida does not supplement the deficiencies of Kono. Tsuchida is relied on to teach a voltage setting circuit for producing a split voltage. Accordingly, Kono and Tsuchida, even when

considered in combination, fail to teach or suggest all limitations of claim 1. For at least this reason, Applicant respectfully requests the withdrawal of rejection of claims 8-10.

Kono and Tsuchida are also not properly combinable for the purpose of this obviousness rejection. There would have been no motivation to combine the references to attain the invention defined by claim 1 absent the improper and impermissible use of hindsight using the present application as a roadmap. The mere fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness, the prior art must also suggest the desirability of the combination, which is not present here. M.P.E.P. § 2143.01 (citing In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990) (emphasis added).

Kono is directed to a method of fabricating a semiconductor memory device with a fuse portion. Tsuchida does not teach or suggest using its voltage setting circuit with the Kono construction. Because of this lack of motivation to combine, independent claim 1 is patentable over these references. For this reason, dependent claims 8-10 are likewise patentable over the references and therefore, Applicant respectfully submits that the 35 U.S.C. § 103 rejection of the claims be withdrawn and the claims allowed.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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